UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,446	01/20/2004	Daniel Frank Moertl	ROC920030380US1	9233

30206 7590 05/12/2006

IBM CORPORATION
ROCHESTER IP LAW DEPT. 917
3605 HIGHWAY 52 NORTH
ROCHESTER, MN 55901-7829

EXAMINER	
SUN, SCOTT C	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 05/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,446	MOERTL ET AL.	
	Examiner	Art Unit	
	Scott Sun	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed 3/16/2006 have been noted and entered. Previous rejections under U.S.C. 112 have been withdrawn.

Response to Arguments

2. Applicant's arguments filed 3/16/2006 have been fully considered but they are not persuasive. Applicant's arguments are summarize as:

a. Prior art of record do not teach nor suggest storing data *and control information* into FIFO.

3. In response to argument 'a', examiner notes that claim 1 recites storing, loading, and outputting control information as intended use, which are functions that the system taught in prior art of record is capable of performing. The intended use of the FIFO as claimed by applicant fails to provide any structural difference between the claimed invention and the prior art of record. One of ordinary skill in the art at the time of invention would readily recognize that FIFO memories could store raw data and control information. For example, control information such as computer instructions executed by processors are conventionally loaded from main memory into a temporary FIFO storage before being run by the processor. As another example, control information can be error correction code used to detect and correct errors (stated in previous rejection; taught by Lee et al). Examiner further notes that control information, as taught by applicant, is used for enabling higher level functions such as DMA and ECC (figure 3;

page 7, lines 12-21), and not to adjust the clock frequency or width of the FIFO. For these reasons, the claimed invention as stated in claims 1 and 16 are not distinguishable from prior art of record.

4. Having addressed each of applicant's arguments, the following rejections are made in response to the newly amended claims.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 5-11, 16-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (PG Pub US 2003/0177295) in view of Chang et al. (US Patent #6,347,380) and Lee et al (PG Pub #US 2004/0093443).

7. Regarding claims 1 and 16, Hsu discloses a flow through asynchronous elastic first-in, first-out apparatus (system in figure 5) comprising: a FIFO RAM having a data input (input port in paragraph 24) for receiving data and control information and a data output (output port in paragraph 24) for outputting said data and control information (column 3, lines 10-15); said FIFO RAM including a plurality of locations for storing a plurality of words, each word including a set number of bits. The examiner notes that by definition computer memory are designed to have memory cells (bits) that form a plurality of words (multiples of 8-bits).

Hsu further discloses a write clocked logic (Wptr in figure 5, paragraph 24) for loading said data and control information to said FIFO RAM at a first clock frequency. Asynchronous read clocked logic (Rptr in figure 5, paragraph 24) for outputting said data and control information from said FIFO RAM at a second clock frequency. The examiner asserts that by definition of asynchronous FIFOs the read and write frequencies are asynchronous to each other. The examiner further notes that claim 1 recites receiving, outputting, and loading of control information are stated as intended use and do not require any structure in the FIFO (see response to arguments above).

Hsu does not disclose explicitly selectively providing one of said second clock frequency and a data width of said FIFO RAM. However, Chang et al discloses a second clock frequency (read frequency) of a FIFO RAM being selectively provided for outputting data and control information from said FIFO RAM with no back pressure (column 6, lines 13-30; column 5, lines 5-7). The examiner notes that Chang discloses the system for adjusting read frequency (output from FIFO) to be higher than write frequency to avoid FIFO overflow (back pressure).

Teachings of Hsu and Chang are from the same field of asynchronous FIFOs. Therefore, it would have been obvious for a person of ordinary skill in the art at the time of invention to combine Chang's and Hsu's teachings by implementing the read frequency adjustment logic disclosed by Chang in the FIFO system of Hsu for the benefit of avoiding FIFO overflow and underruns (Chang, column 5, lines 5-7).

Regarding claim 16, examiner notes that various transfers of control information are stated as a functional limitations rather than intended use as in claim 1.

Accordingly, in anticipation of applicant's amending claim 1 to explicitly perform the functions as in claim 16, the following additional rejection is applied.

Hsu and Chang combined do not disclose control data being transferred through the FIFO. However, Lee teaches that data packets stored in FIFOs contain both data and control information (packet header, ECC; paragraph 2, 74). Teachings of Hsu, Chang, and Lee are from the same field of FIFOs.

Therefore, it would have been obvious at the time of invention for a person of ordinary skill in the art to combine teachings of Hsu and Chang, and further with teachings of Lee by storing both data and control information in the FIFO for the benefit of performing ECC to maintain data integrity and enable higher level functions (paragraph 74, 76).

8. Regarding claim 2, Hsu, Chang, and Lee combined disclose claim 1, and Chang further discloses wherein said FIFO RAM includes a multiple location FIFO RAM used on each asynchronous boundary. The examiner asserts that Chang discloses the FIFO interfaces between different write and read frequencies (Codec clock and host USB clock; column 3, lines 16-39), which are asynchronous boundaries.

9. Regarding claim 5, Hsu, Chang and Lee combined disclose claim 1, and Lee further discloses wherein said data and control information includes a control field storing parity or ECC control information (paragraph 74).

10. Regarding claim 11, Hsu, Chang, and Lee combined disclose claim 1, and Hsu further discloses wherein said write clocked logic for loading said data and control information to said FIFO RAM at said first clock frequency includes a Gray code

increment block encoding a write address input to said FIFO RAM (Wmaster in figure 4, paragraph 24).

11. Regarding claims 6-9, Hsu, Chang, and Lee combined disclose claim 1 but do not disclose explicitly using data and control field to select and write data to a target engine. However, the examiner asserts that a person of ordinary skill in the art at the time of invention would readily recognize that data transferred have control information (for example the header of a packet) indicating the destination, including engine and buffer, of the data.

12. Regarding claim 10, Hsu, Chang, and Lee combined disclose claim 1 but do not disclose explicitly using control field to authorize for discarding data. However, the examiner asserts that a person of ordinary skill in the art at the time of invention would readily recognize that data no longer needed such as data containing errors are discarded. For example, Lee teaches that data in a FIFO is discarded (deleted) after an error is found (figure 8). The examiner further asserts that a person of ordinary skill in the art would readily recognize that some type of data (for example, 1 bit in the header of data packet) is used to mark (authorize) a packet of data for discarding.

13. Regarding claims 17-23, the examiner asserts that these claims are substantially similar to claims 1, 5-10. Specifically, claim 17 is similar to claim 1, claim 18 is similar to claim 8, claim 20 is similar to claim 6, claim 21 is similar to claim 7, claim 22 is similar to claim 9, claim 19 is similar to claim 10 and claim 23 is similar to claim 5. They are rejected using the same arguments. They are rejected using the same arguments.

14. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu in view of Chang and Lee and further in view of Adamchick (US Patent #4,122,520).

Hsu, Chang, and Lee combined disclose claim 1 but do not disclose explicitly using DMA. However, Adamchick discloses using a DMA system (figure 3a). It would have been obvious for a person of ordinary skill in the art at the time of invention to combine Adamchick's teachings with teachings of Hsu, Chang, and Lee by using DMA, as disclosed by Adamchick, to direct data transfer through the FIFO RAM system disclosed by the combined teachings Hsu, Chang, and Lee for the benefit of altering the contents of a memory without altering the speed of CPU (column 1, lines 6-10). The examiner further asserts that the use of DMA to direct data transfer has been well known for many forms of data transfer in general, and that a person of ordinary skill in the art would readily recognize that DMA can be used to direct data transfer through a FIFO RAM.

15. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu in view of Chang and Lee and further in view of Lowe et al (US Patent #6,937,172).

16. Regarding claim 12, Hsu, Chang, and Lee combined disclose claim 11 discloses Gray code increment block but do not disclose explicitly a multiplexer coupled to said Gray code increment block. However, Lowe discloses a multiplexer coupled to a Gray code increment block (figure 9D) and receiving a write strobe select input (step 998,

pointer increment assertion) for incrementing a Gray code write address (step 997). Lowe's teachings and teachings of Hsu, Chang, and Lee are from analogous art of FIFOs (see Lowe's background).

Therefore, it would have been obvious at the time of invention to combine Lowe's teachings with combined teachings of Hsu, Chang, and Lee by adding the multiplexers disclosed by Lowe into the combined system of Hsu, Chang, and Lee for the benefit of selecting a between incremented value and a register value (column 13, lines 43-48).

17. Regarding claim 13, Hsu, Chang, Lee, and Lowe combined disclose claim 12, and Hsu further discloses a pair of synchronization latches to provide a synchronization input to said asynchronous read clocked logic for outputting said data and control information from said FIFO RAM at said second clock frequency (synchronization circuits in figure 6, paragraph 24). The examiner notes that Hsu discloses the sync circuits can be flip-flops (which are latches).

18. Regarding claim 14 and 15, the examiner asserts that Hsu further discloses the write and read Gray code circuits are identical (last line of paragraph 2). Therefore the same arguments used in rejection of claims 11 and 12 are used.

Conclusion

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Sun whose telephone number is (571) 272-2675. The examiner can normally be reached on M-F, 10:30am-7pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KIM HUYNH
SUPERVISORY PATENT EXAMINER
5/3/06